

**AMENDMENTS TO THE CLAIMS**

1. (Currently Amended) A method for analyzing power in a component comprising:
  - determining a plurality of current densities, wherein each current density is associated with one portion of a plurality of portions of the component;
  - determining a plurality of wire densities, wherein each wire density is associated with one region of a plurality of regions of the component; and
  - comparing the plurality of current densities and the plurality of [[power]] wire densities.
2. (Original) The method of claim 1, further comprising:
  - determining a ratio of the plurality of current densities and the plurality of wire densities; and
  - identifying any geometric coordinates whereby the ratio exceeds a predetermined number.
3. (Original) The method of claim 1, further comprising:
  - selecting the component from the group consisting of:
    - a processor, a memory chip, a memory controller chip, a chipset component, a communications chip, a graphics chip, a VLSI component, and a computer component.
4. (Original) The method of claim 1, further comprising:
  - forming a plot of a ratio of the plurality of current densities and the plurality of wire densities.
5. (Original) The method of claim 4, further comprising:
  - associating the plot with a portion of a design of the component.

6. (Original) The method of claim 1, wherein determining the plurality of current densities comprises:

determining a respective current consumption value for a plurality of elements within the one portion of the component; and

mapping the plurality of current consumption values to geometric coordinates for a design of the component.

7. (Original) The method of claim 6, wherein the step of determining a respective current consumption value comprises:

calculating  $CVf(A_f)$ ;

wherein C is a capacitance of the element, V is a voltage of the element, f is the clock frequency of the element, and  $A_f$  is the activity factor of the element.

8. (Original) The method of claim 6, wherein the plurality of elements are field effect transistors.

9. (Original) The method of claim 6, wherein the elements are connected to a power wire.

10. (Original) The method of claim 6, wherein mapping the plurality of current consumption values comprises:

translating the geometric coordinates to a level of the design that corresponds to a level of analysis for the analyzing power in the component.

11. (Original) The method of claim 1, wherein determining a plurality of wire densities comprises:

repeating a window across a portion of the design of the component;

determining a density of power wires within each window; and

mapping the plurality of power wire densities to geometric coordinates for the design of the component.

12. (Original) The method of claim 11, wherein determining a plurality of wire densities further comprises:

selecting a size of the analysis window.

13. (Original) The method of claim 12, wherein the design is a hierarchical design that has a plurality of hierarchical levels, the method further comprises:

increasing the size of the window as a level of interest of the hierarchical design is increased.

14. (Original) The method of claim 11, wherein mapping the plurality of current consumption values comprises:

translating the geometric coordinates to a level of the design that corresponds to a level of analysis for the analyzing power in the component.

15. (Original) The method of claim 11, further comprising:

overlapping the windows to form average values for the wire densities.

16. (Original) The method of claim 1, wherein the design has a plurality of power wire levels, and determining a plurality of wire densities further comprises:

summing the plurality of power wire levels to a single level.

17. (Currently Amended) The method of claim 1, wherein the design has a plurality of power wire levels, and determining a plurality of wire densities further comprises:

determining a plurality of wire densities for each level of the design; and

comparing the plurality of current densities and the plurality of [[power]] wire densities for each level of the design.

18. (Original) The method of claim 1, wherein the design is a hierarchical design that has a plurality of hierarchical levels, the method further comprises:

flattening the hierarchical design into a single level.

19. (Original) The method of claim 1, wherein determining a plurality of wire densities comprises:

(a) sliding a window across a portion of a region of the design of the component;

(b) determining a density of power wires within each window;

repeating (a) and (b) for the region of the design; and

mapping the plurality of power wire densities to geometric coordinates for the design of the component.

20. (Currently Amended) A system for current management comprising:  
means for determining a plurality of current densities of a component;  
means for determining a plurality of wire densities of the component; and  
means for forming a comparison of the plurality of current densities and the plurality  
of [[power]] wire densities.

21. (Currently Amended) A computer program product for current management  
having a computer readable medium, the product comprising:

code, that is stored on the computer readable medium, for determining a plurality of  
current densities of a component;

code, that is stored on the computer readable medium, for determining a plurality of  
wire densities of the component; and

code, that is stored on the computer readable medium, for forming a representation of  
the plurality of current densities and the plurality of [[power]] wire densities that is viewable  
by a user.